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ABSTRACT OF THE DISCLOSURE

A plurality of sub word lines each have a length equivalent to the division of a main word line along the extension direction thereof, arranged along a bit line crossing said main word line, and are connected with a plurality of memory cells. A first sub word select line arranged in parallel to the main word line is extended to a plurality of sub arrays arranged in the extension direction of the word line. A second sub word select line is connected to the corresponding one of said first sub word select line to be extended orthogonally to a word line driving circuit area of an adjacent sub array. In the sub word line driving circuit provided for each sub array, a sub word line is selected and deselected by signals supplied from said main word line and said second sub word select line.